XRM-OPT

High Speed Serial Adaptor Module

User Guide

Version 1.10

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EMI

This equipment generates, uses and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference if not installed and used with adequate EMI protection for specific applications.

Caution

This equipment uses Class 1 Laser devices; such devices are not considered to be hazardous when used for their intended purpose. Use of controls, adjustments or performance of procedures other than those specified herein may result in hazardous laser light exposure.

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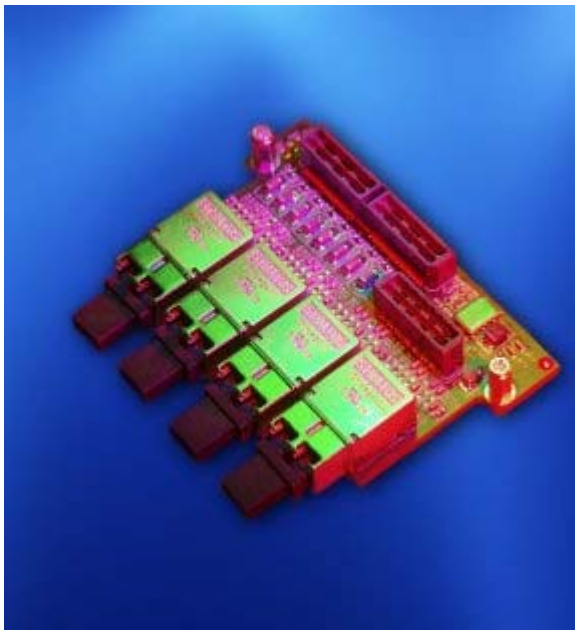


1. Introduction

The XRM-OPTO is a front-panel adapter card designed for use with Alpha Data's PMC cards. These include the ADM-XP, XRC4FX, XRC5T1 and XRC5T2.

Low-profile Copper/Optical transceivers are used to provide external connectivity to a number of the Multi-Gigabit Transceivers (MGTs) on the FPGA. The XRM-OPTO allows easy connection of these cards to devices with compatible transceivers by means of simple, point-to-point connection schemes implemented using off-the-shelf optical fibre.

Configuration options include Singlemode (1310nm) or Multimode (850nm) operation and bit rates from 155 Mbaud to 3.125 Gbaud.

A dedicated low-jitter oscillator is provided to support high-bit rate applications.

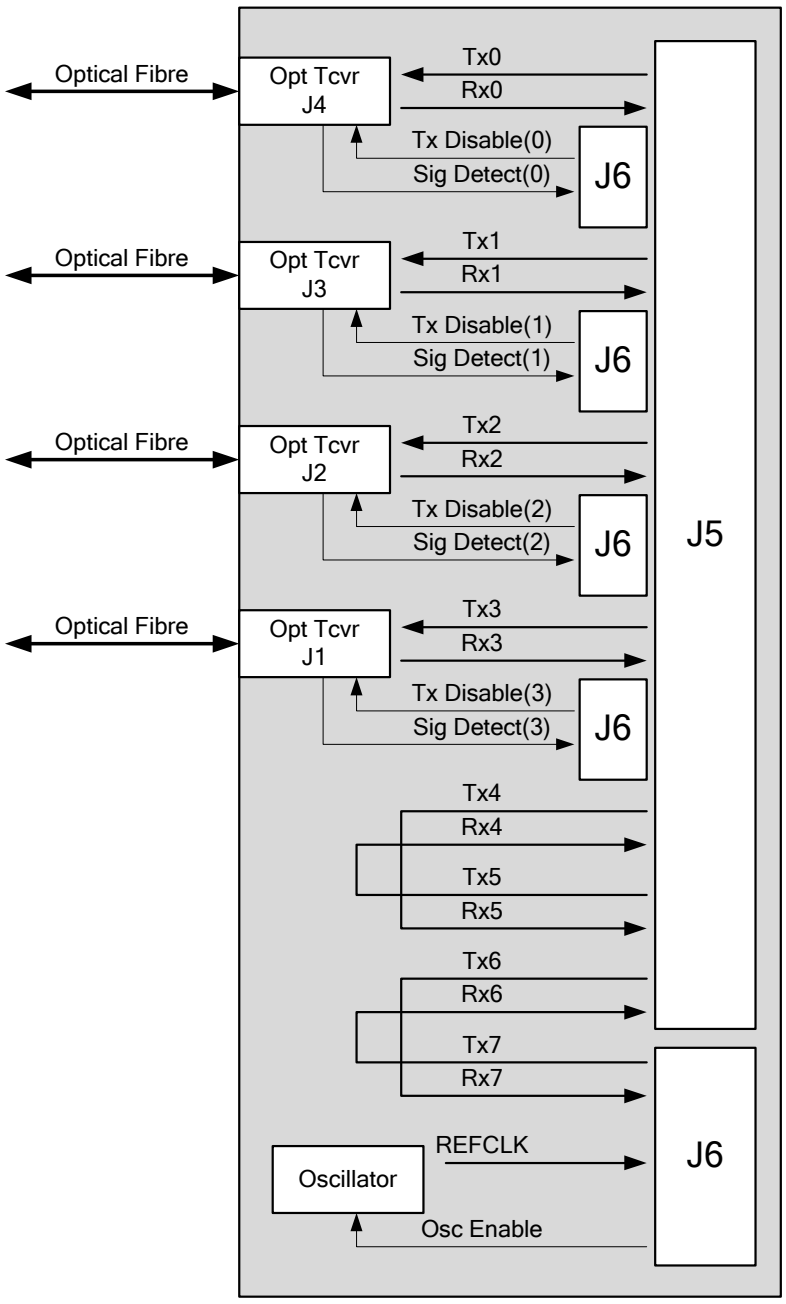


Figure 1 XRM-OPTO Block Diagram

2. Installation

The XRM-OPTO is designed to plug in to the front panel connectors (SAMTEC QSE-DP and QSH series) on Alpha Data's range of FPGA PMC cards.

The retaining screws should be tightened to secure the XRM- OPTO to the FPGA card.

Notes:
The control signals on the XRM-OPTO use LVTTL (3.3V) signalling levels. The XRM I/O Voltage on the PMC card must be set to 3.3V

This operation should not be performed while the PMC card is powered up.

2.1. Handling instructions

Observe precautions for preventing damage to components by electrostatic discharge. Personnel handling the board should take SSD precautions. Avoid flexing the board.

3. Specification

3.1. Mating Cables

Mating cables require the use of 'LC' style connections with appropriate wavelength characteristics and length.

3.2. Ordering Info

Boards can be ordered populated with 1 to 4 transceivers, in specific board sites if required.

A number of combinations of baud rate, distance, optical mode and optical wavelength are available. Standards include GigE/FC, Fast Ethernet, Infiniband, 1x/2x FibreChannel, Pixel Bus and OC3/STM1.

The frequency of the on-board oscillator to suit the application should also be specified. For Virtex4 and Virtex 5 boards, this normally requires that the appropriate wizard is run from the Xilinx tools to determine the correct frequency because of the clocking options on these devices.

Virtex2 Pro boards normally require a frequency of 0.05 * the bit rate.

Contact the factory for further details.

4. Related Documents

ADM-XP User Manual
ADM-XRC4FX User Manual
ADM-XRC5T1 User Manual
ADM-XRC5T2 User Manual

5. Design Examples

Example designs or starting points of an application for the XRM-OPT are available using the Xilinx CORE Generator included in the ISE tool set.

After creating a CORE Generator project for the FPGA card being used with the XRM-OPT the appropriate Wizard for the serial interface will be enabled in the 'IO Interfaces' section of the 'FPGA Features and Design' IP group, as shown below.

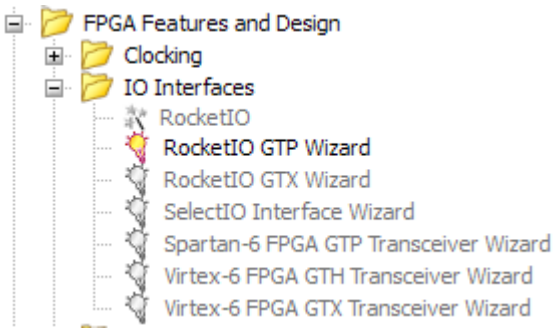


Figure 2 Wizard selection in CORE Generator

6. Pinout

UCF Name	Samtec Pin	XP	4FX	5T1	5T2	Dir	Function	Note
txp<0>	J5-1	A40	A36	U2	AA2	Out	J4 Tx	
txn<0>	J5-3	A41	A37	T2	Y2	Out	J4 Tx	
rxp<0>	J5-2	A39	C39	T1	Y1	In	J4 Rx	
rxn<0>	J5-4	A38	D39	R1	W1	In	J4 Rx	
txp<1>	J5-5	A36	A34	M2	T2	Out	J3 Tx	
txn<1>	J5-7	A37	A35	N2	U2	Out	J3 Tx	
rxp<1>	J5-6	A35	A31	N1	U1	In	J3 Rx	
rxn<1>	J5-8	A37	A32	P1	V1	In	J3 Rx	
txp<2>	J5-17	A8	P39	L2	R2	Out	J2 Tx	
txn<2>	J5-19	A9	R39	K2	P2	Out	J2 Tx	
rxp<2>	J5-18	A7	U39	K1	P1	In	J2 Rx	
rxn<2>	J5-20	A6	V39	J1	N1	In	J2 Rx	
txp<3>	J5-21	A4	M39	F2	K2	Out	J1 Tx	
txn<3>	J5-23	A5	NE9	G2	L2	Out	J1 Tx	
rxp<3>	J5-22	A3	J39	G1	L1	In	J1 Rx	
rxn<3>	J5-24	A2	K39	H1	M1	In	J1 Rx	
sig_detect<0>	J6-2	C13	L28	AA10	J38	In	Signal detect	
sig_detect<1>	J6-4	D13	K28	AB10	K38	In	Signal detect	
sig_detect<2>	J6-6	H13	J29	AA8	K40	In	Signal detect	
sig_detect<3>	J6-8	G13	H24	AA9	K39	In	Signal detect	
tx_disable<0>	J6-1	D10	C27	AP14	Y34	Out	Output disable	
tx_disable<1>	J6-3	E10	C28	AN14	AA34	Out	Output disable	
tx_disable<2>	J6-5	F11	L29	AM13	W35	Out	Output disable	
tx_disable<3>	J6-7	E11	K29	AN13	Y35	Out	Output disable	
osc_enable	J6-106	L27	AC25	H20	L30	Out	Output disable	1
brefck_in_p	J6-109	G22	F39	E4	C4	In	Ref Clock	2
brefck_in_n	J6-111	F22	G39	D4	C3	In		2
txp<4>	J5-9	BB4	AT39	E2	J2	Out	Loopback to Rx5	3
txn<4>	J5-11	BB5	AU39	D2	H2	Out	Loopback to Rx5	3
rxp<4>	J5-10	BB3	AW37	D1	H1	In	Loopback from Tx5	3
rxn<4>	J5-12	BB2	AW36	C1	G1	In	Loopback from Tx5	3
txp<5>	J5-13	BB8	AP39	B4	D2	Out	Loopback to Rx4	3
txn<5>	J5-15	BB9	AR39	B3	E2	Out	Loopback to Rx4	3
rxp<5>	J5-14	BB7	AL39	A3	E1	In	Loopback from Tx4	3
rxn<5>	J5-16	BB6	AM39	A2	F1	In	Loopback from Tx4	3
txp<6>	J5-25	BB36	AW25	B5	B1	Out	Loopback to Rx7	3
txn<6>	J5-27	BB37	AW24	B6	B2	Out	Loopback to Rx7	3
rxp<6>	J5-26	BB35	AW22	A6	A2	In	Loopback from Tx7	3
rxn<6>	J5-28	BB34	AW21	A7	A3	In	Loopback from Tx7	3
txp<7>	J6-117	BB40	AW28	B10	B6	Out	Loopback toRx6	3
txn<7>	J6-119	BB41	AW27	B9	B5	Out	Loopback to Rx6	3
rxp<7>	J6-118	BB39	AW31	A9	A5	In	Loopback from Tx6	3
rxn<7>	J6-120	BB38	AW30	A8	A4	In	Loopback from Tx6	3

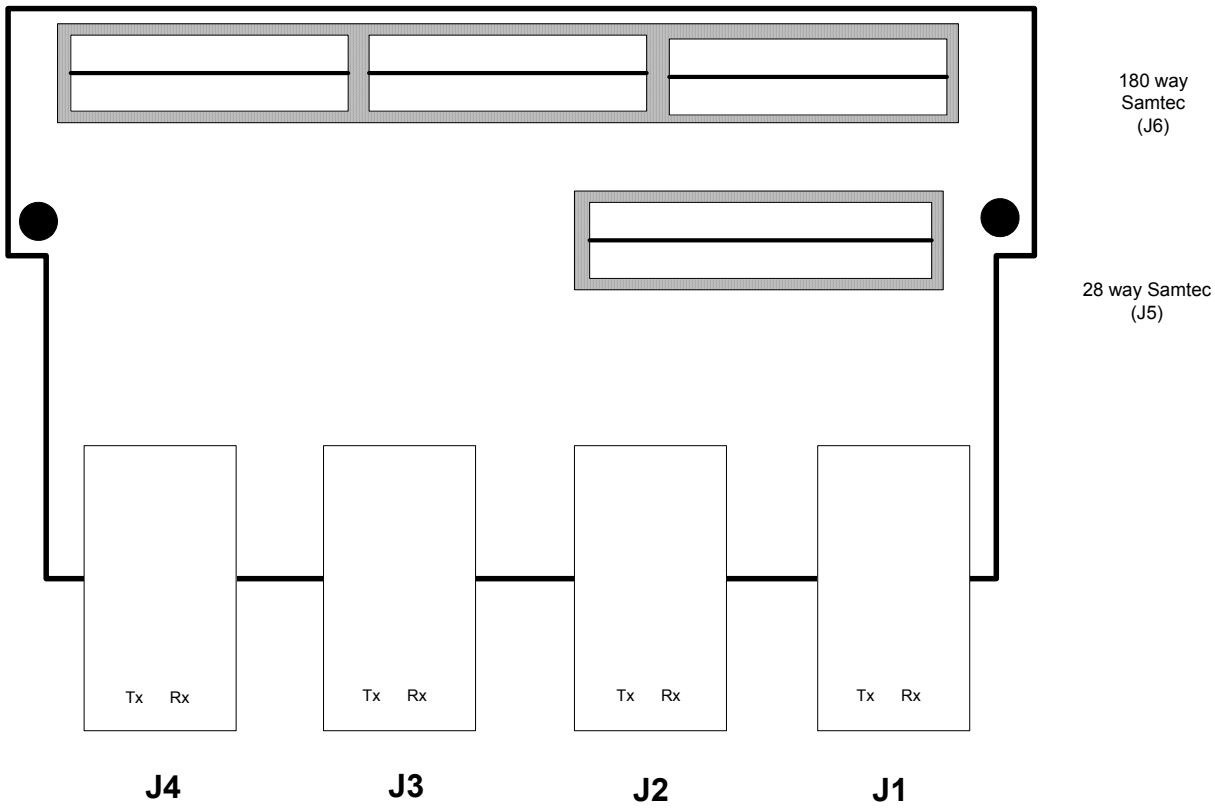
Notes

(1) Oscillator Enable should use “open-collector” output drive on FPGA. Drive ‘0’ to disable oscillator, High-Z to enable oscillator.

(2) For ADM-XRC-XP applications, BREFCLK_P is connected to P6-97, BREFCLK_N is connected to P6-99.

(3) Loopback connections are not accessible externally.

7. Board Layout



7.1. MGT Mappings

J4= UCF channel 0
J3= UCF channel 1
J2= UCF channel 2
J1= UCF channel 3

UCF channels 4 and 5 connected internally for loopback.
UCF channels 6 and 7 connected internally for loopback.

Revision History

Date	Revision	Nature of Change
Feb-2005	1.0	Initial draft
Jan-2006	1.1	Corrected minor typos.
Oct-2007	1.2	Added Tx/Rx indication
Dec08	1.3	Added 4FX documentation
Dec 08	1.4	Added 5T1, 5T2 documentation
Apr 09	1.5	Corrected clock pins for 4FX, 5T1, 5T2
June 09	1.6	Revised block diagram. Samtec pin numbers added. Added note on I/O voltage settings.
June 09	1.7	Changed Samtec references from “P” to “J”, increased maximum line rate to 3.125Gb/s.
June2009	1.8	Corrected 5T2 pinouts; J1, J2 pins (UCF channels 2,3) swapped with pins for UCF channels 4 and 5. Added note regarding oscillator frequencies in ordering information.
Nov 2009	1.9	Changed XRM-OPTO references to XRM-OPT. Added notes about using CORE Generator for example code.
June 2010	1.10	Corrected connectivity in block diagram